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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,503	10/16/2001	L. James Hwang	X-953 US	6920

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EXAMINER	
BRODA, SAMUEL	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,503	HWANG ET AL.	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-9 and 11-14* is/are rejected.

7)☒ Claim(s) *2-5 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined.

Drawings

2. Applicants' formal drawings have been reviewed and approved.

Claim Rejections - 35 U.S.C. § 112, Second Paragraph

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3.1 Claims 11-14 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are the hardware components necessary to operate each limitation that together form the "system."

Claim Rejections - 35 U.S.C. § 101

4. The following is a quotation of 35 U.S.C. 101:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4.1 System claims 11-14 are rejected for reciting a machine that appears to be implemented in software alone, thus not being tangible and forming the basis of statutory subject matter under 35 U.S.C. 101.

In each of claims 11-14, the system is claimed in terms of "design objects" and an "environment" that together form the "apparatus." Absent the computer hardware necessary to create the design objects and environment to create the electronic circuit design, the system claims appear incomplete and thus not tangible under Section 101.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> . . .
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.1 Claims 1, 6-9, and 11 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Krukowski et al, "Simulink/Matlab-to-VHDL Route for Full-Custom/FPGA Rapid Prototyping of DSP Algorithms," Matlab DSP Conference, pp. 1-10 (November 1999)(text available at: http://dolphin.wmin.ac.uk/~artur/pdf/Paper18.pdf).

5.2 Regarding claims 1, 9, and 11, Krukowski et al teaches a bit-true hardware implementation using a "Simulink-to-VHDL converter" using Matlab and s-functions. This

implementation is identical to the implementation described in Applicants' Specification. See Abstract, page 1 and pages 4-9 describing the automatic generation of a two-path two-coefficient polyphase filter in VHDL from a Simulink design.

5.3 Regarding 6-8, Krukowski et al teaches the use of testbench construction to compare the VHDL simulation results to the output of Simulink. See Section 2.7 "Conversion of the Model to VHDL" pages 9-10.

Allowable Subject Matter

6.1 Claims 2-5 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6.2 Claims 12-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. {101, 112 second paragraph}, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Reference to Schaumont et al, U. S. Patent 6,606,588 is cited as teaching a design apparatus for generating an implementable description of a digital system.

Reference to Graef, U. S. Patent 6,305,001 is cited as teaching a clock distribution network planning and method.

Reference to Ito et al, U. S. Patent 6,216,255 is cited as teaching a computer-aided logic circuit designing system including a clock system analyzing section.

Reference to Rompaey et al, U. S. Patent 5,870,588 is cited as teaching a design environment for hardware/software co-design.

Reference to Garbergs et al, "Implementation of a State Space Controller in a FPGA," IEEE 9th Mediterranean Electrotechnical Conference, Vol. 1, pp. 566-569 (May 1998), is cited as teaching a control system design implemented in Simulink connected to a hardware design implemented in VHDL via ASCII files.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (571) 272-3709. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (571) 272-2100.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER